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| MEMORIES | 210688 |
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| <u>L19</u> | (disabl\$4 or enabl\$4 or activat\$5) near8 (sub near2 group\$4 or plur\$7 or multipl\$6 or group\$4 or set\$1 or sub neal set\$1 or two) near7 memory near3 bank\$1 near12 (simultaneous\$3 or concurrent\$3) | 130 | <u>L19</u> |
| <u>L18</u> | L14 and cache\$1 | 11 | <u>L18</u> |
| <u>L17</u> | L16 and cache\$1 | 1 | <u>L17</u> |
| <u>L16</u> | (disabl\$4 or enabl\$4 or activat\$5) near5 (plur\$7 or multipl\$6 or group\$4 or set\$1 or sub neal set\$1 or two) near5 memory near3 bank\$1 near7 (simultaneous\$3 or concurrent\$3) | 82 | <u>L16</u> |
| <u>L15</u> | (disabl\$4 or enabl\$4 or activat\$5) near8 (plur\$7 or multipl\$6 or group\$4 or set\$1 or sub neal set\$1 or two) near7 memory near3 bank\$1 near7 (simultaneous\$3 or concurrent\$3) | 119 | <u>L15</u> |
| <u>L14</u> | (disabl\$4 or enabl\$4 or activat\$5) near8 (plur\$7 or multipl\$6 or group\$4 or set\$1 or sub neal set\$1 or two) near7 memory near3 bank\$1 near12 (simultaneous\$3 or concurrent\$3) | 130 | <u>L14</u> |
| <u>L13</u> | L12 not l11 | 1 | <u>L13</u> |
| <u>L12</u> | (disabl\$4 or enabl\$4 or activat\$5) near8 (plur\$7 or multipl\$6 or group\$4 or set\$1 or sub neal set\$1 or two) near7 memory near3 bank\$1 near16 cache\$1 | 23 | <u>L12</u> |
| <u>L11</u> | (disabl\$4 or enabl\$4) near8 (plur\$7 or multipl\$6 or group\$4 or set\$1 or sub neal set\$1 or two) near7 memory near3 bank\$1 near16 cache\$1 | 22 | <u>L11</u> |
| <u>L10</u> | (disabl\$4 or enabl\$4) near8 (group\$4 or set\$1 or sub neal set\$1 or two) near7 memory near3 bank\$1 near16 cache\$1 | 5 | <u>L10</u> |
| <u>L9</u> | (disabl\$4 or enabl\$4) near8 (group\$4 or set\$1 or sub neal set\$1) near7 memory near2 bank\$1 near16 cache\$1 | 3 | <u>L9</u> |
| <u>L8</u> | (disabl\$4 or enabl\$4) near8 (group\$4 or set\$1 or sub neal set\$1) near7 memory near2 bank\$1 near9 cache\$1 | 3 | <u>L8</u> |
| <u>L7</u> | (disabl\$4 or enabl\$4) near4 (group\$4 or set\$1 or sub neal set\$1) near5 memory near2 bank\$1 near9 cache\$1 | 1 | <u>L7</u> |
| <u>L6</u> | (disabl\$4 or enabl\$4) near4 (group\$4 or set\$1 or sub neal set\$1) memory near2 bank\$1 near9 cache\$1 | 120312 | <u>L6</u> |
| <u>L5</u> | (disabl\$4 or enabl\$4) near4 memory near2 bank\$1 near9 cache\$1 | 36 | <u>L5</u> |
| <u>L4</u> | (disabl\$4 or enabl\$4) and l3 | 3 | <u>L4</u> |
| <u>L3</u> | L2 near12 instruction\$1 near4 cache\$1 | 3 | <u>L3</u> |
| <u>L2</u> | (disabl\$4 or enabl\$4) near4 memory near2 bank\$1 | 1071 | <u>L2</u> |
| <i>DB=USPT; PLUR=YES; OP=OR</i> | | | |
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







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